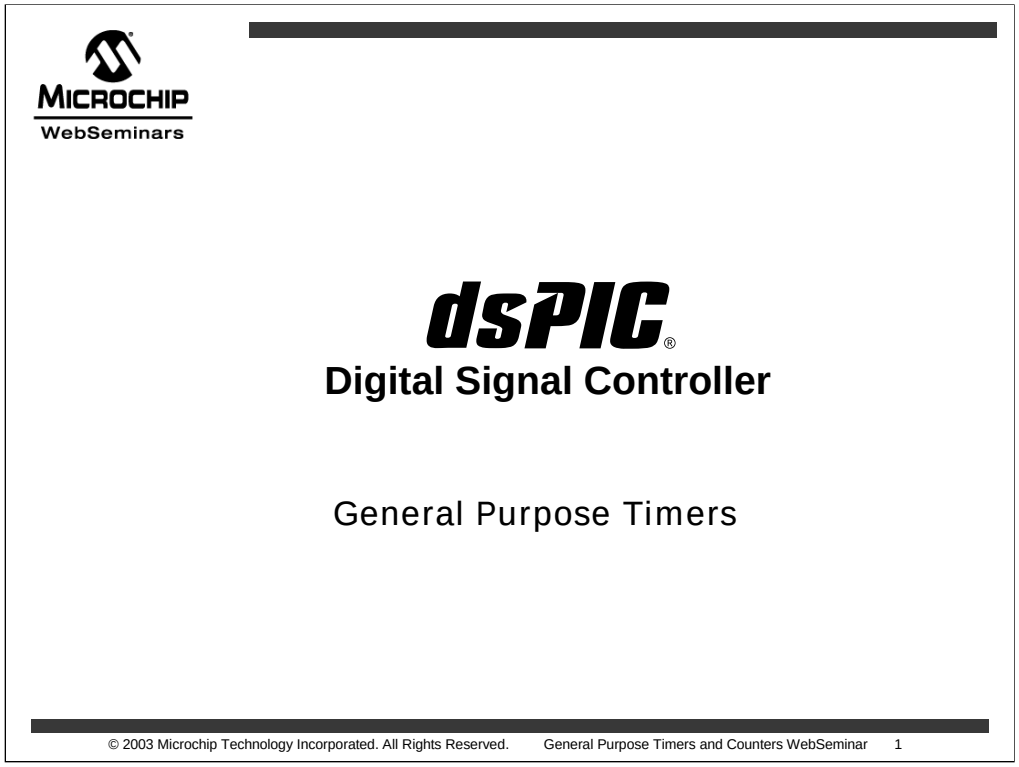
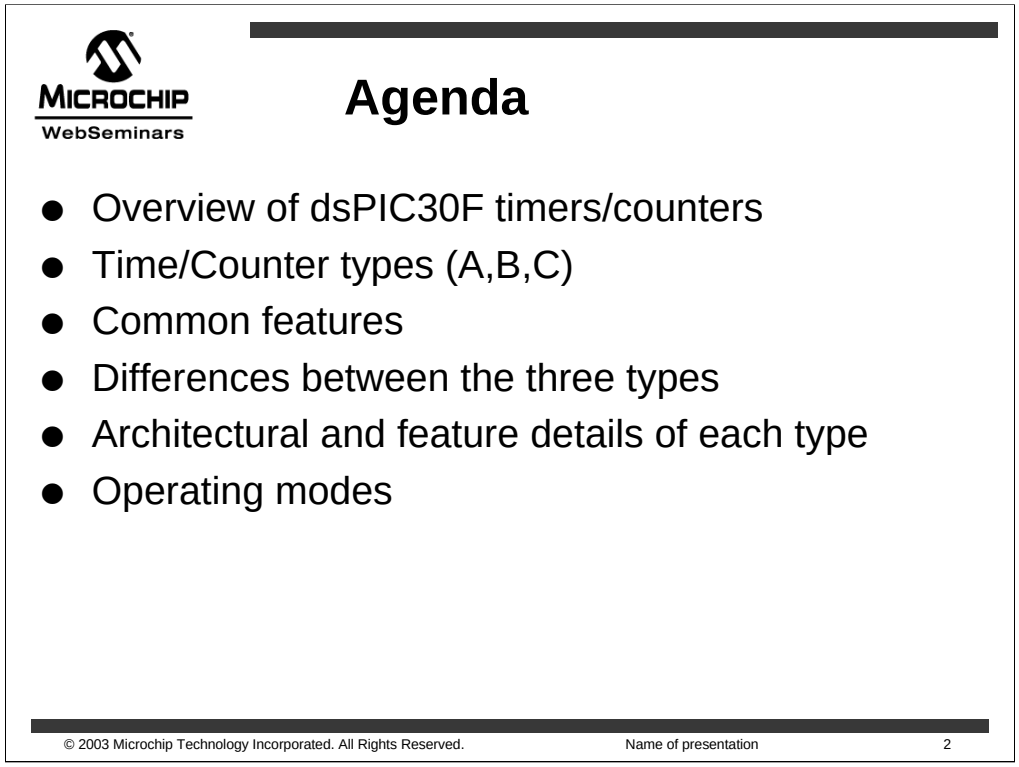


Hello, and welcome to another in the series of dsPIC digital signal controller (DSC) web-based training seminars by Microchip.

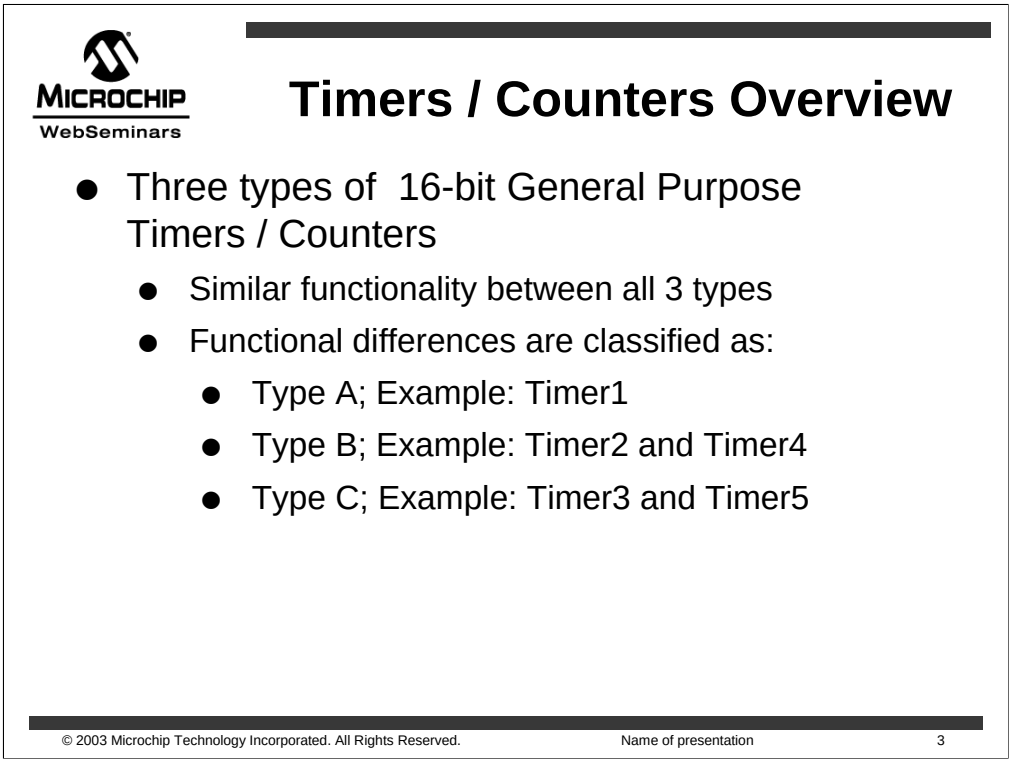
Today we will be looking at the General Purpose timers offered as peripheral modules on the dsPIC30F family of microcontrollers.

I hope you find this helpful in your understanding of the dsPIC30F product family.

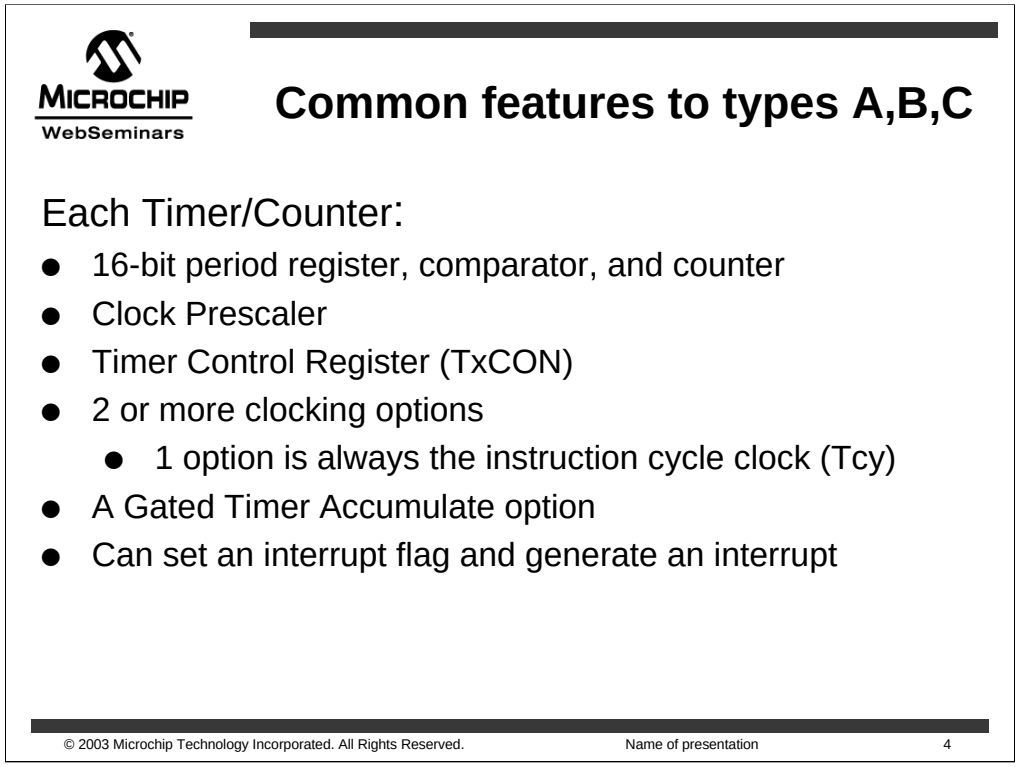


We will discuss the features of each of the three different types of general purpose timers available on the dsPIC30F.

This discussion will be followed by details on the various operating modes of the Timer's and how they may be configured to operate in each mode.



A brief overview of the timers. There are 3 different types of general purpose 16-bit timers that are available on dsPICs. Their basic functionality is similar but there are a few differences. To note these differences, the timers are classified as Type A, Type B and Type C. Timer 1 is a Type A, Timers 2 and 4 are Type B and Timers 3 and 5 are Type C. Depending on which dsPIC device you choose you will have either 3 or 5 timers available.



Most of the building blocks of all 3 types are the same.

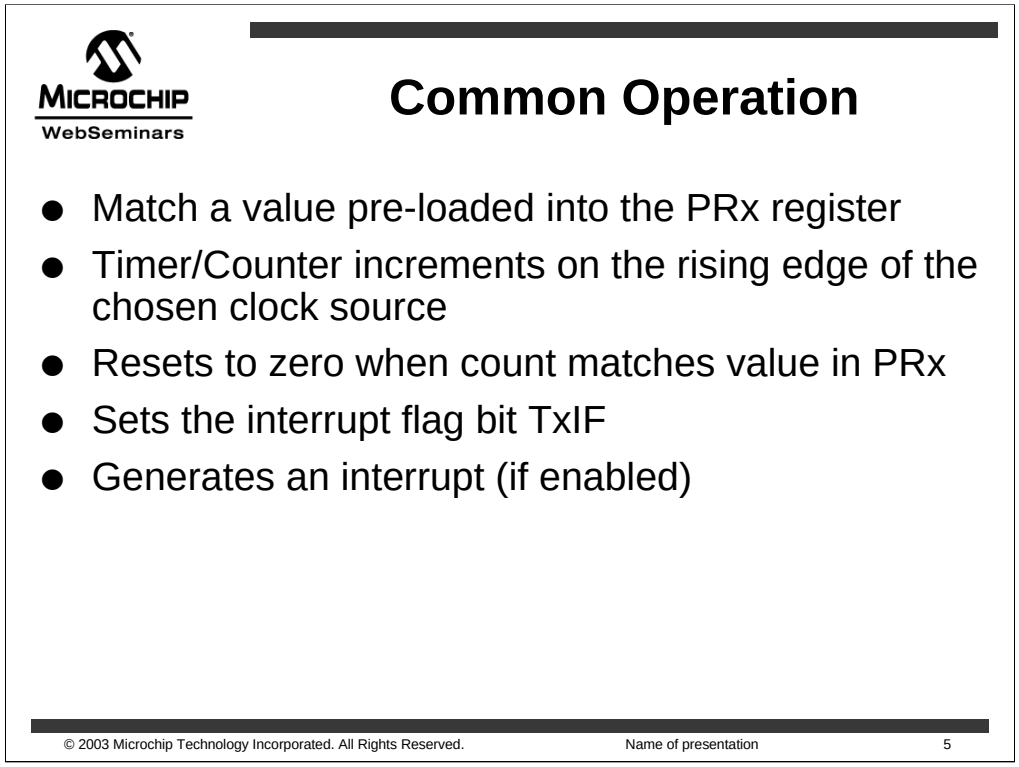
Each timer has its own Period Register, comparator, counter, prescaler, and control register.

Each timer has an option of using either the internal instruction cycle clock or an external clock source.

A gated time accumulate mode also exists on all timers. In this mode the timers can count how long the Timer Clock input pin was pulsed high or low.

All three types of timers can all set an interrupt flag and generate an interrupt on reaching a certain count held in the Period register.

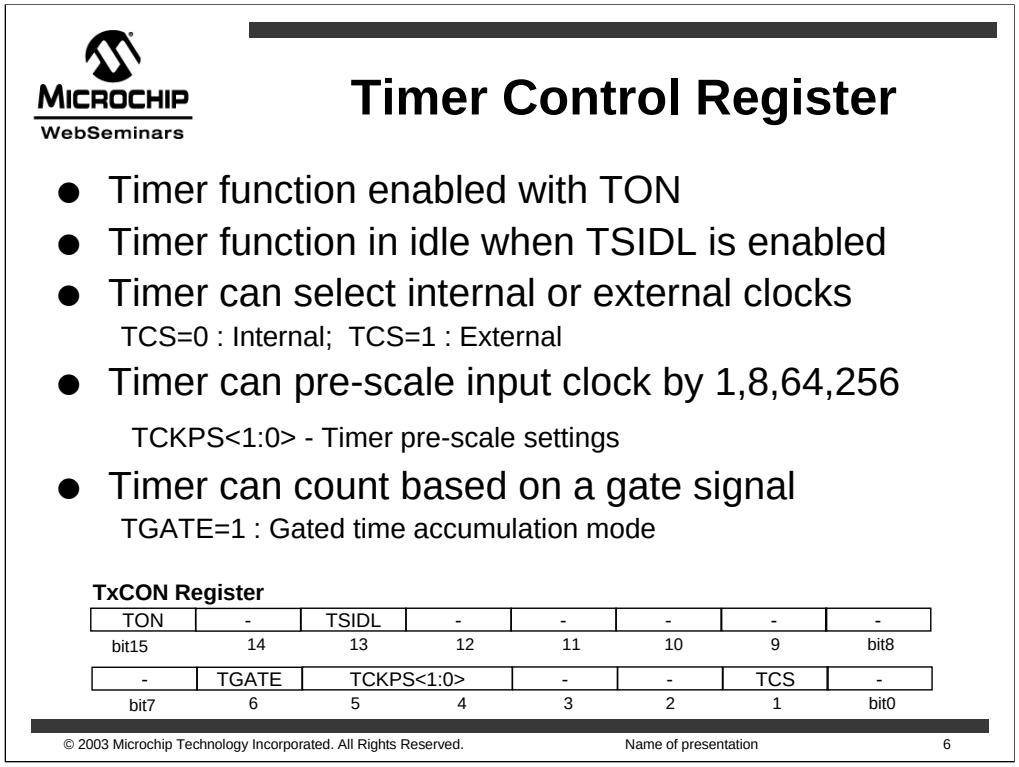
We will go over the basic timer operation, next.



The operation of the timers is straight forward.

A 16 bit match value is loaded into the associated period register and the timer/counter is enabled.

The counter increments on each rising edge of the chosen clock source. When the comparator detects it has reached a match with the period register the interrupt flag is set, an interrupt is made if enabled, and the counter is reset to zero and the whole process starts again.



Each Timer has its own control register called TxCON, shown at the bottom of the screen, where x stands for the timer number. The bit definitions are as follows:

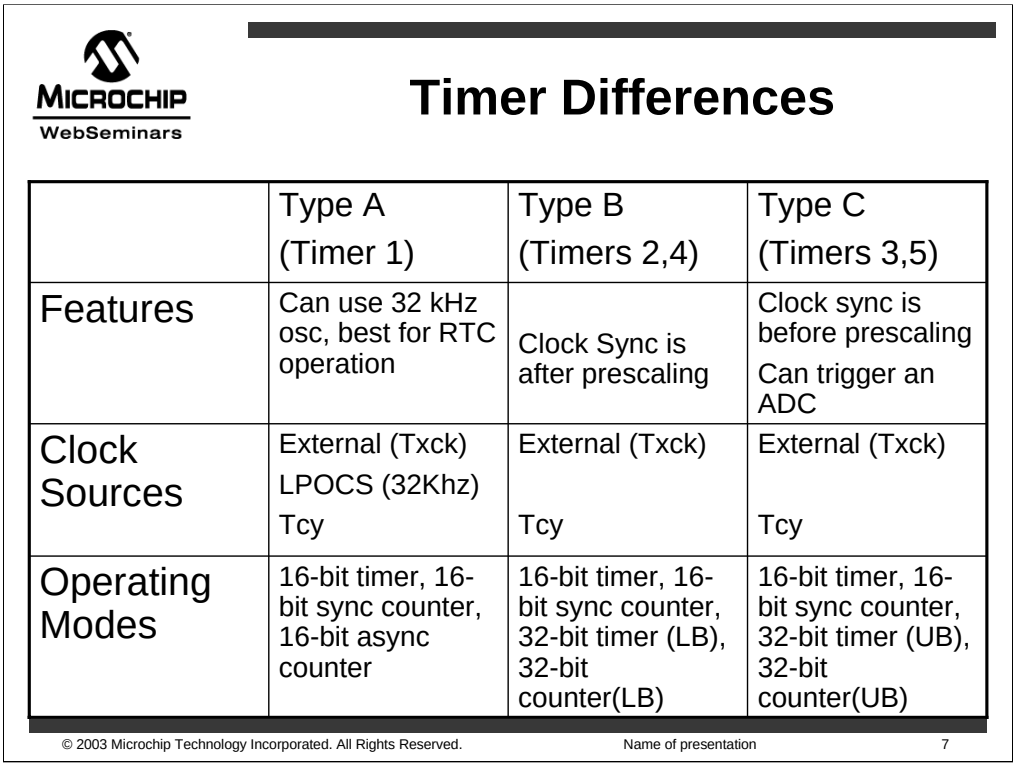
TON turns ON or starts the timer when set to 1

TSIDL when set to 1 allows the operation of the timer in idle mode

TCS when set to 1 selects the external clock, when cleared to 0 the internal clock is selected.

TCKPS bits select the pre-scale value used to divide an incoming frequency by 1, 8, 64 or 256

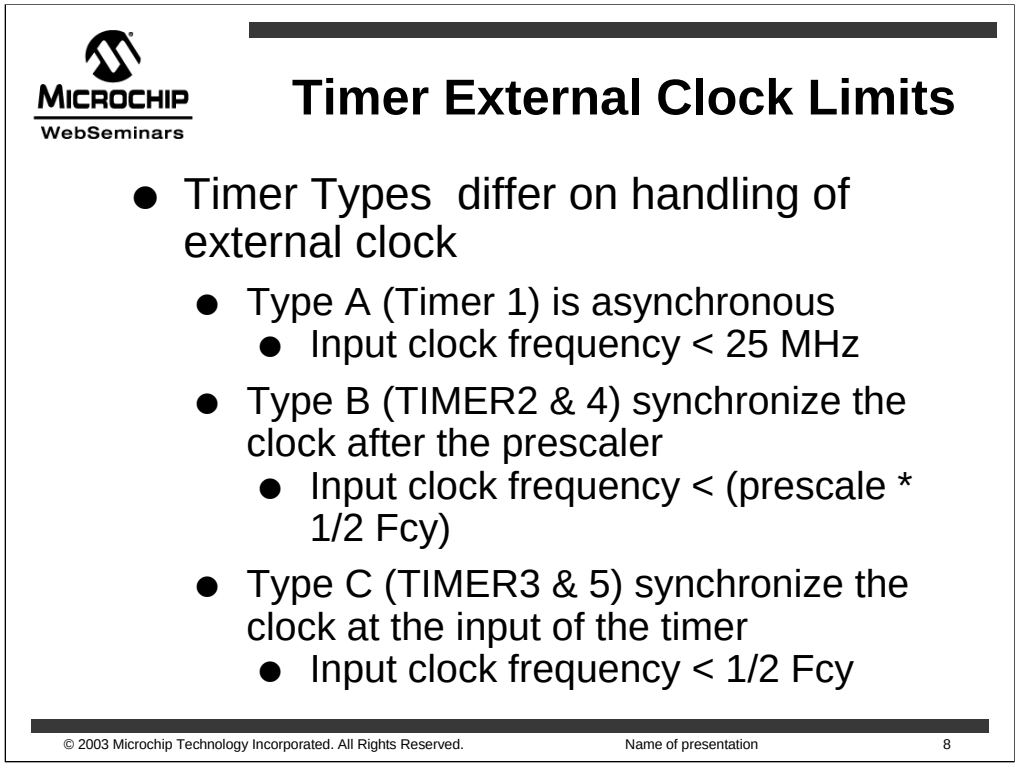
TGATE when set to 1 enables the gated time accumulate mode, we will discuss this in detail later



Here is a snapshot of the differences between the three types of timers :

As you can see, Timer 1 may be used as a real-time clock as it accepts an asynchronous 32 KHz external crystal as an input clock.

Also, Timer2 and Timer3 as well as Timer4 and Timer5 may be paired up to form 32-bit timers.



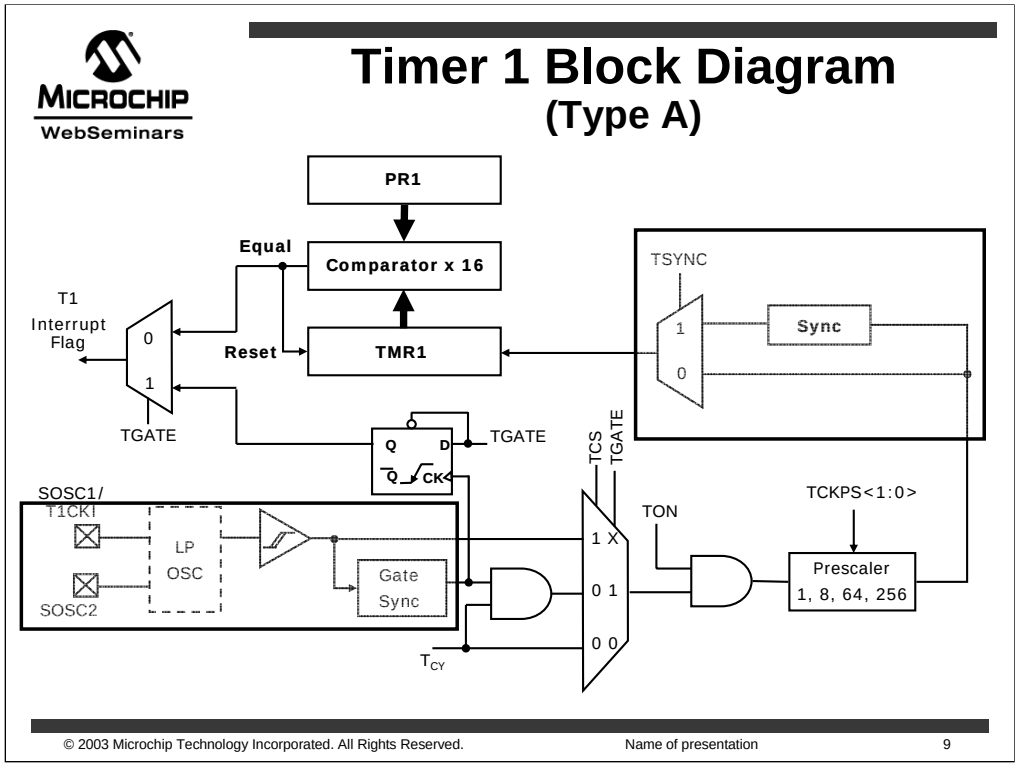
Timers differ on how they handle or count external clock signals.

Type A timer or Timer 1 is the only asynchronous timer. The maximum input signal rate is 25 megahertz This restriction is mainly due to the asynchronous gating logic on Timer 1.

Type B timers, timers 2 and 4 are synchronous timers, however their synchronizing circuit is positioned after the prescaler hence the maximum input clock frequency should be less than half internal instruction cycle frequency (Fcy) times the prescale value

Type C timers or timers 3 and 5 have their synchronizing circuit at the input, so the maximum input clock frequency should be less than half Fcy.

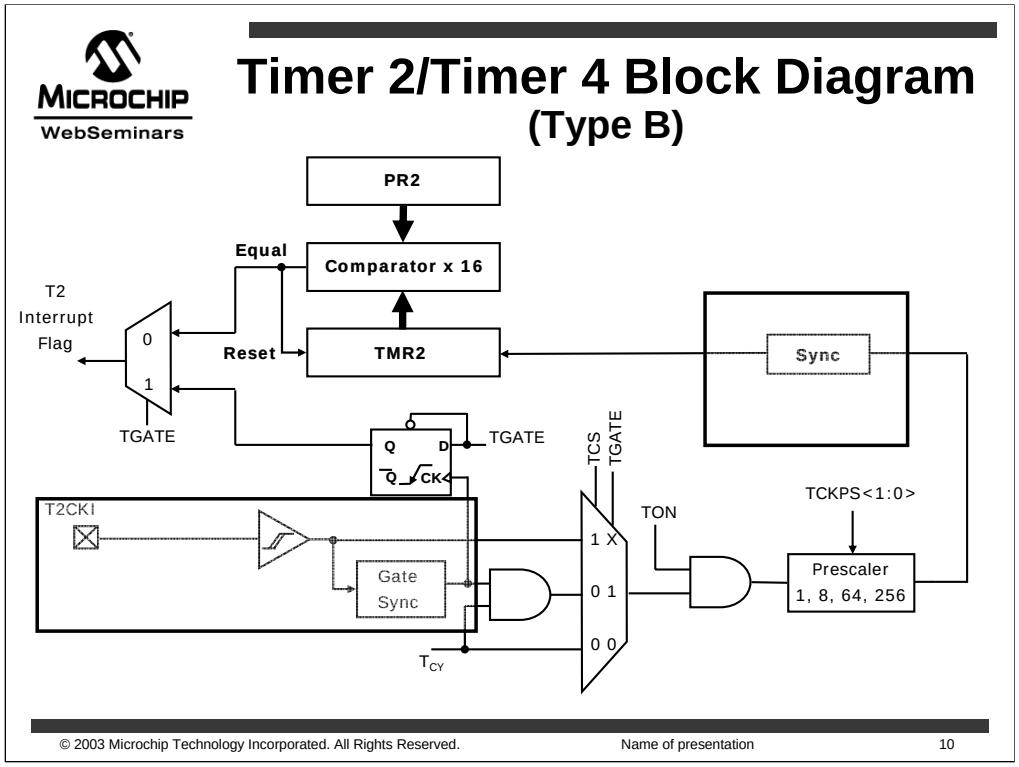
In all the above cases the minimum rise and fall time of the input circuit should not be violated. The minimum rise or fall time in the data sheet is 10 nanoseconds maximum or 50 Mega hertz input frequency.



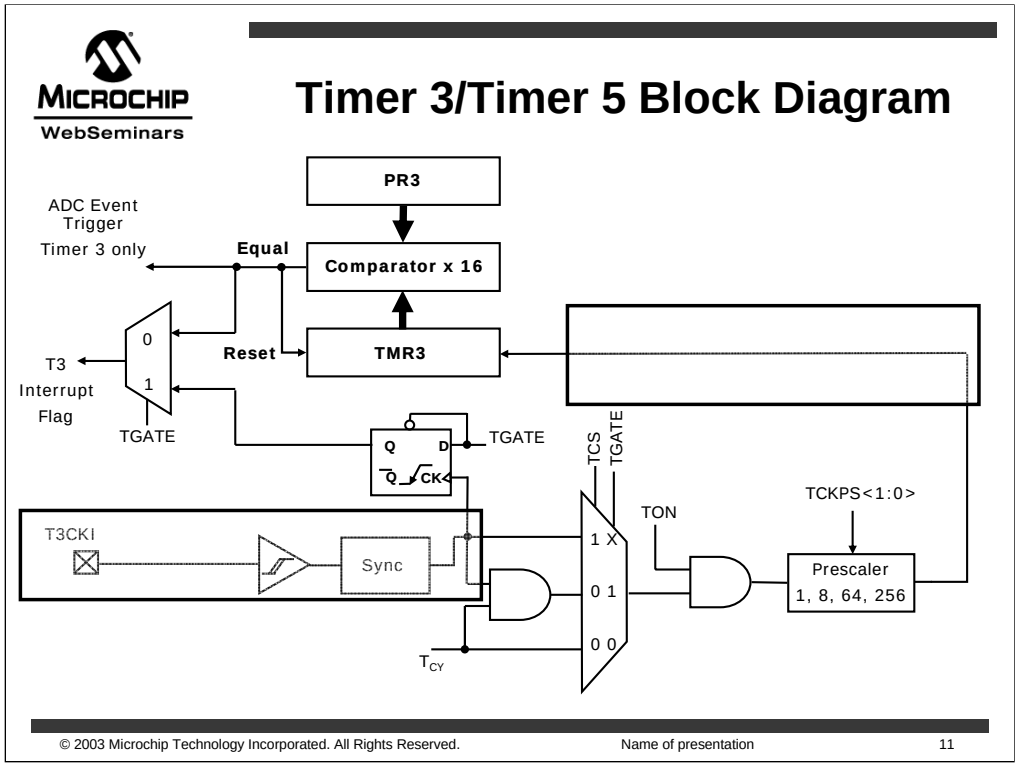
Let us briefly describe Timer 1, which is the only Type A timer. The shaded area highlight where the differences between each type exist.

It's main feature is that it can be used asynchronously. That is, this timer can operate or count without the system clock being active. Thus this feature allows the timer to operate in sleep mode. Another important feature on the Type A timers is that it has the option of being connected to a 32Khz crystal. An Low Power oscillator circuit is available which converts the crystal signal to a pulse which can be counted by the timer. This timer can operate in sleep mode and is very well suited for real time clock applications.

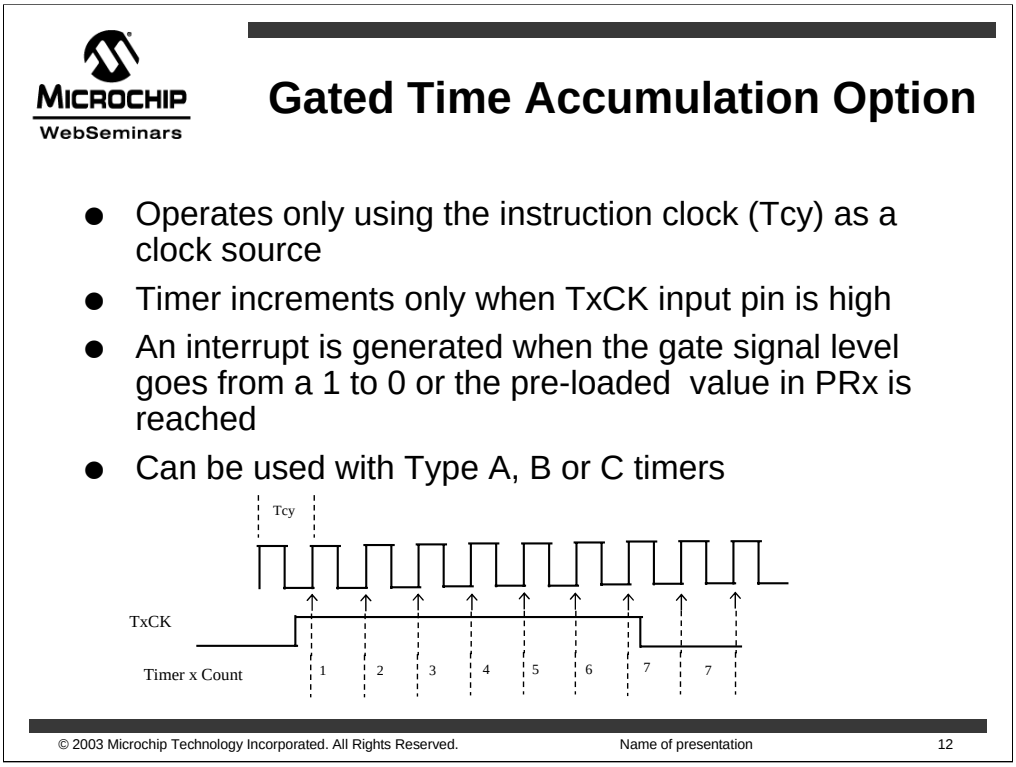
This timer can also be used synchronously. The synchronizing circuit is after the prescaler hence a higher frequency than the internal clock freq. can be counted by timer 1.



This block diagram is for Timer 2 which is a Type B. The key item to note is that the synchronization circuit is located after the pre-scaler hence a frequency higher than Fcy can be measured using this timer. Also notice that the 32KHz crystal is not an option for a clock source for this timer.

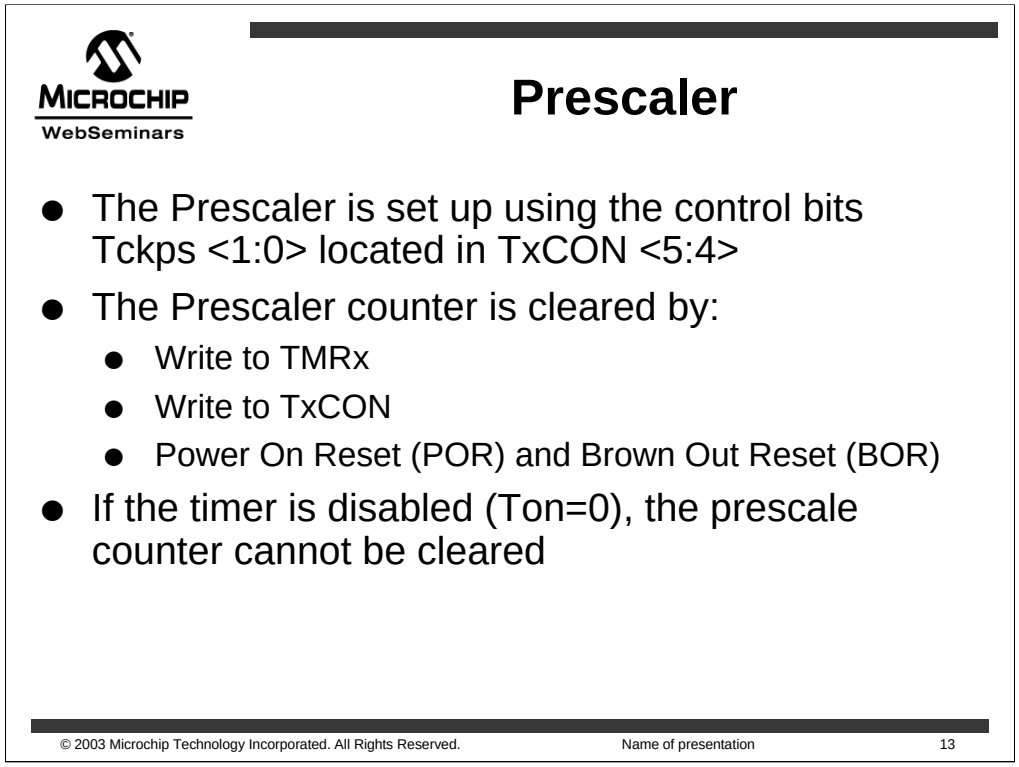


Timer 3 is a Type C timer. This timer is a synchronous timer in which the incoming clock signal is immediately synchronized to the system clock and then measured. If the frequency being measured is less than the instruction clock Fcy then this process will not give rise to any error in measurement. One other feature in Type C timers is the ADC event Trigger. Type C timers can be set to generate a trigger which signals the ADC to begin a conversion. Note that this feature is only available on Timer 3. We will go over each operating mode in detail later.



Type A, B and C have a gated time accumulation option.

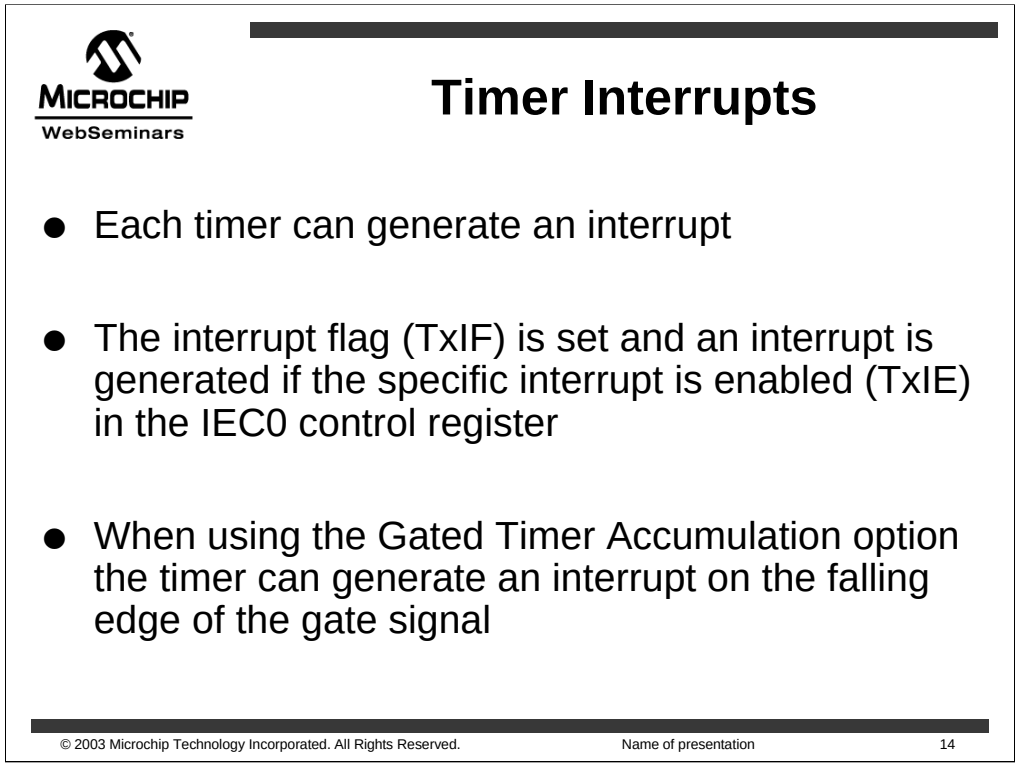
If the unknown frequency is supplied to the TxCK pin as the gating pulse then so long as the level on the pin is high, the value in the Timer is incremented every rising edge of Tcy. Once the level goes from a high to a low, the counting is stopped and an interrupt is generated to signal that this event has occurred. During the interrupt service routine, the user can read the timer value and clear it for another operation.



The input clock to the timer has a prescale option of 1:1, 1:8, 1:64, or 1:256. This is selected by control bits Tckps 1 and 0. These are located in the associated TxCON register bits 5 and 4.

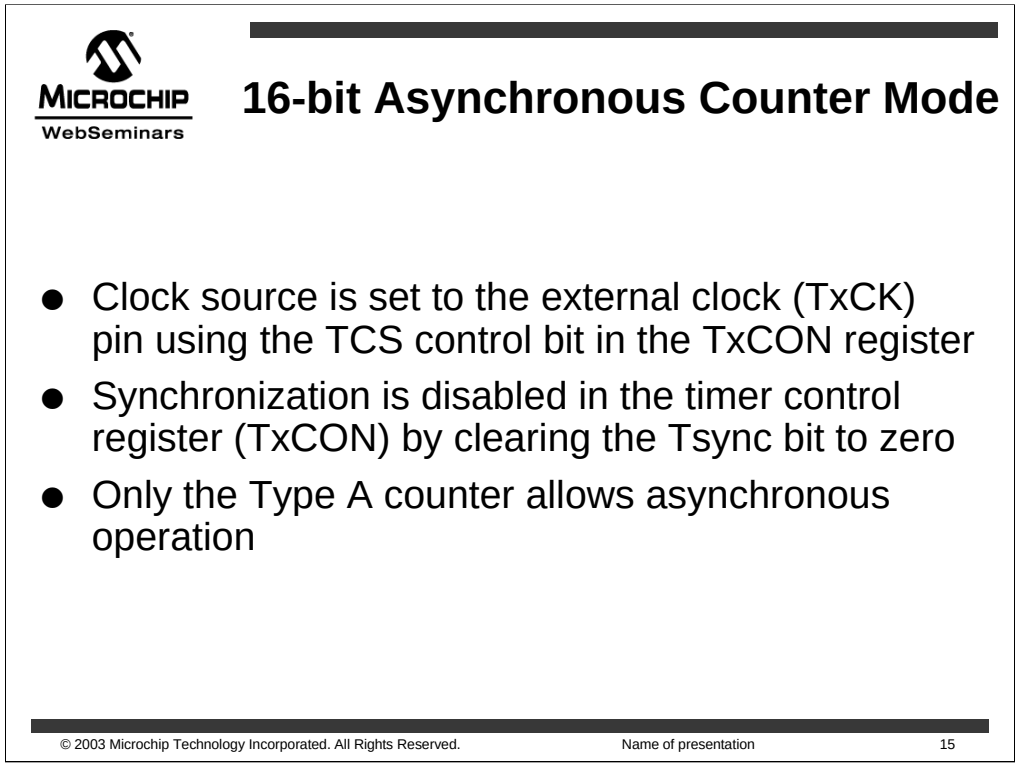
The prescaler counter is cleared with any write to the associated timer register, timer control register, a power on reset, or a brown out reset.

Note however, if the Ton bit is disabled, there is no clock to the prescaler counter and it can not be cleared.

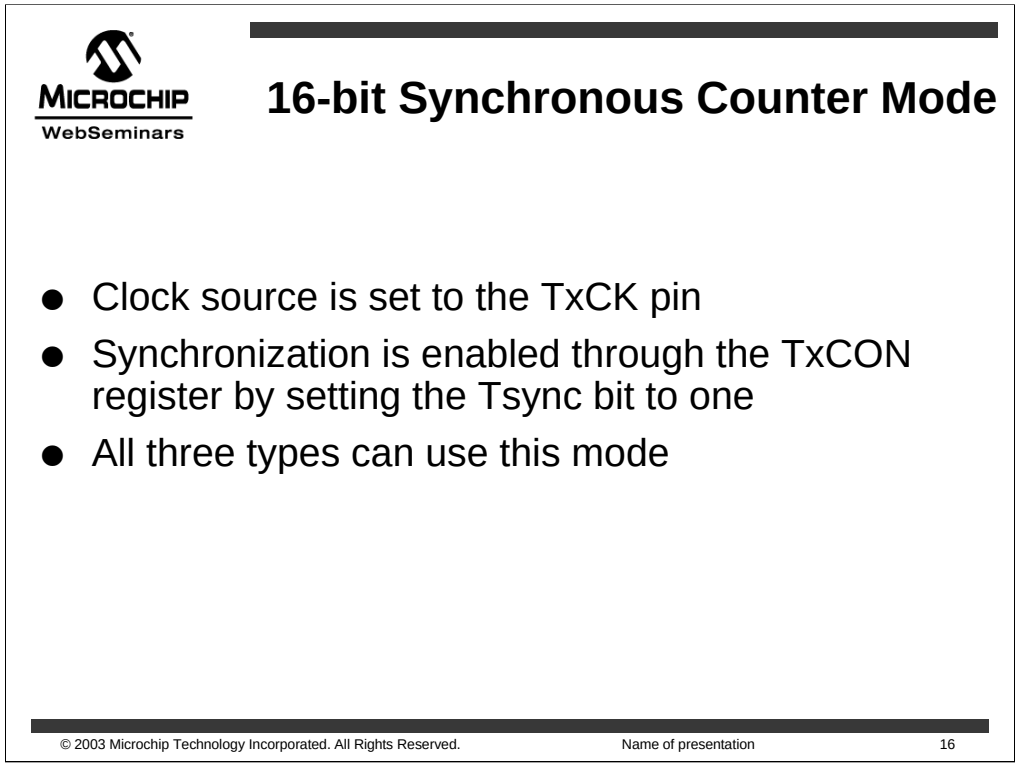


The timer has the ability to generate an interrupt on period match. When the timer count matches the period register, the timer interrupt flag bit (TxIF) is set and a interrupt will be generated if enabled. Enabling the interrupt is accomplished by setting the respective TxIE bit in the interrupt control register.

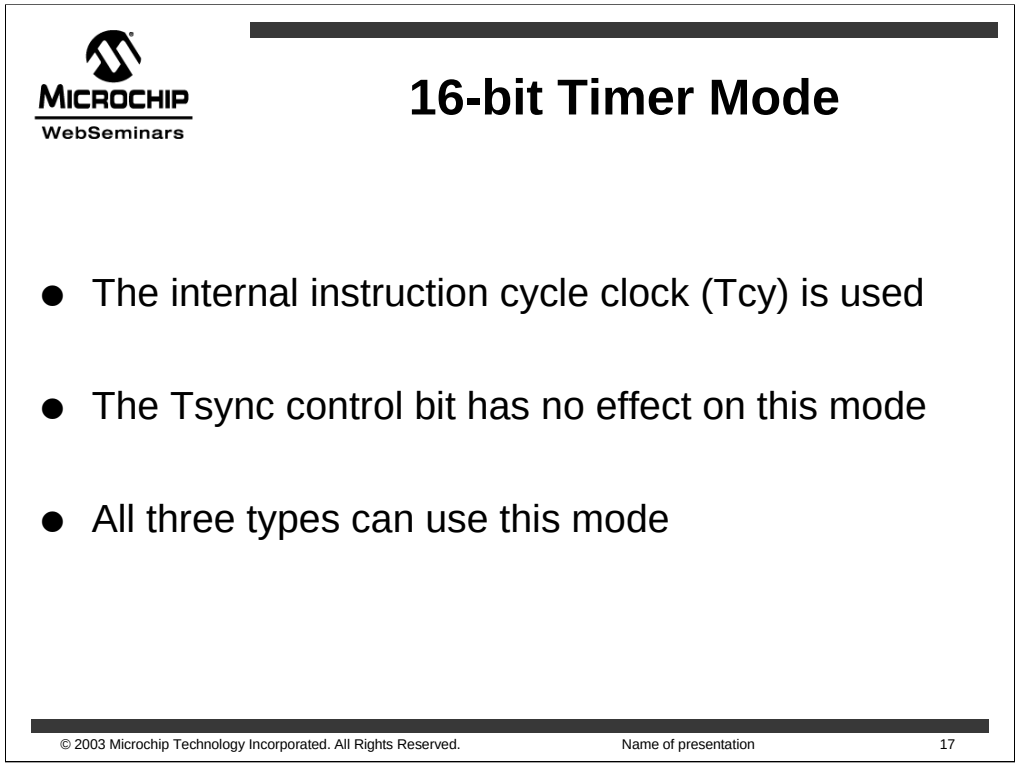
When the Gated timer Accumulate option is used, an interrupt can also be generated on the falling edge of the gate signal.



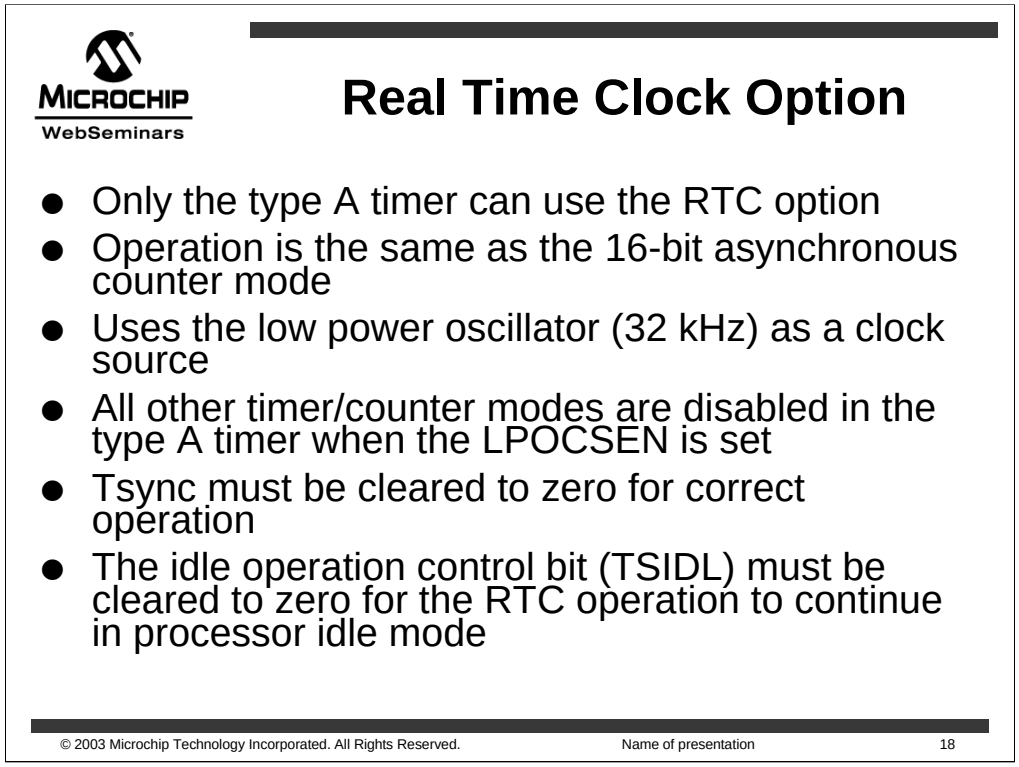
Asynchronous counter mode increments the counter on each rising edge of an external clock. Synchronous mode must be disabled in the timer control register. This is an option only with Timer 1 which is the Type A timer/counter.



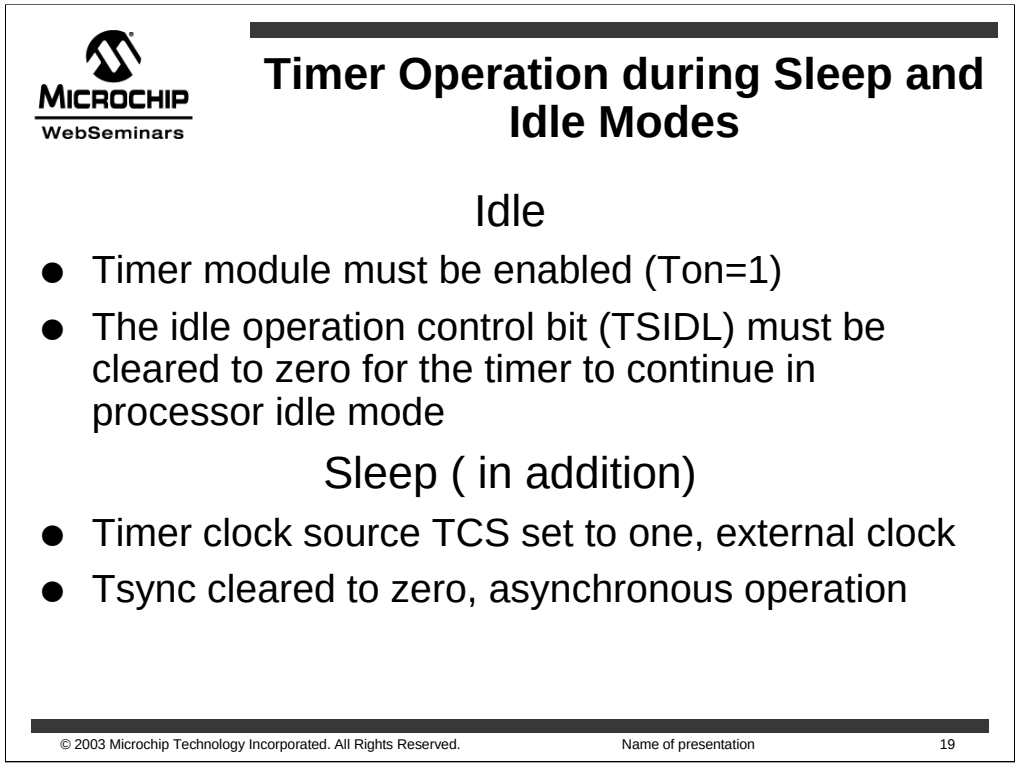
Synchronous operation is the same except internally the rising edge of the external clock is synchronized with the internal instruction cycle clock. All 3 types can use this mode.



In the 16 bit timer mode, the timer increments on every instruction cycle up to a match value preloaded into the period register, then resets to zero and continues to count. The Tsync bit has no effect and this mode is available on all 3 type timers.

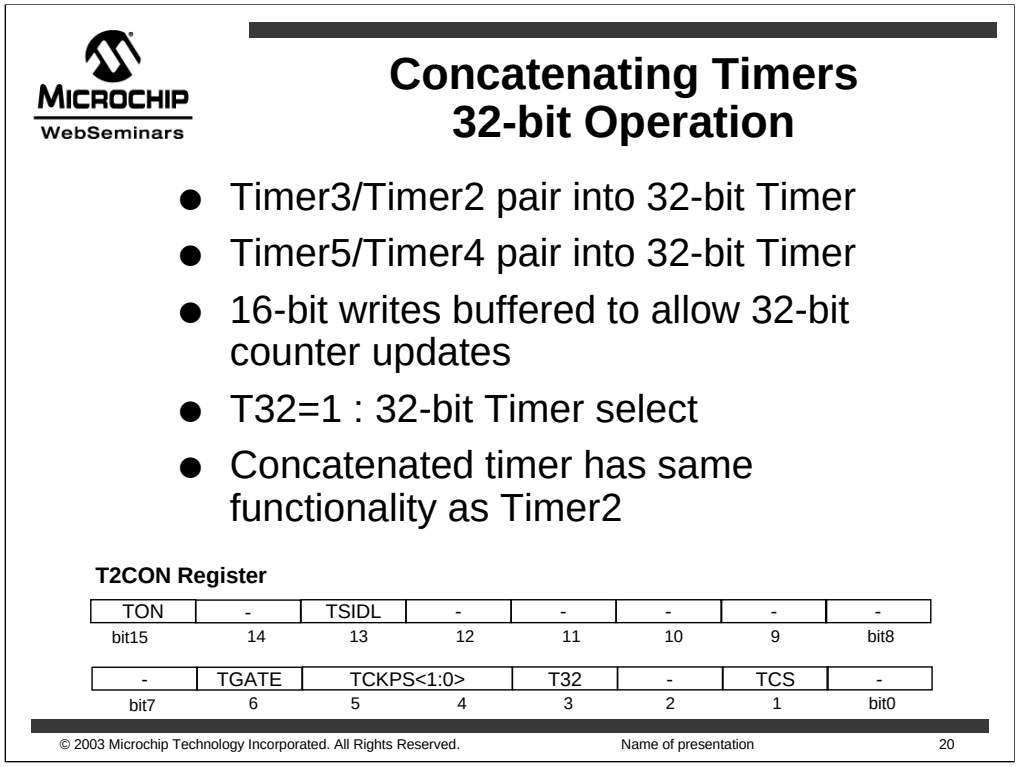


Real time clock is a special option on type A timers. By enabling the low power oscillator this timer will accept a slow 32KHz input. Other that the ultra slow clock source the operation is identical to the asynchronous mode we discussed earlier. No other timer/counter operation is available on type A timers if the low power oscillator is enabled. The Tsync bit must be disabled for RTC operation. If you want the RTC to continue to work while the processor is in IDLE mode then Tsidl must be cleared.



Any time a timer/counter is to continue operation while the processor is IDLE Tsidl must be cleared. Also anytime you want a timer to operate the Ton bit has to be set.

In addition the those two control bits, if you want a timer to operate when the processor is in SLEEP mode you must have the Tsync bit cleared for asynchronous operation because the internal instruction cycle clock is off in sleep mode. Also, the clock source must be external.



In some applications very large counts are required, hence it is important to concatenate two 16 bit registers.

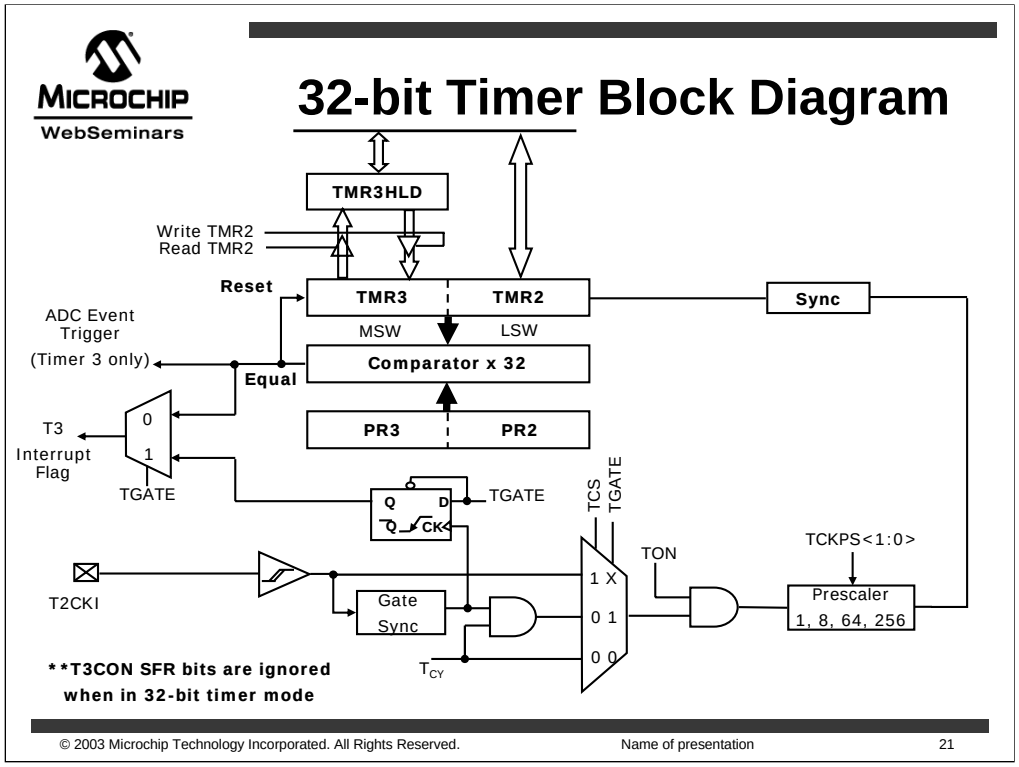
Only type B and Type C timers can be concatenated

Timer 3 can be concatenated with Timer 2 to form a 32 timer

Timer 5 can be concatenated with Timer 4 to form a 32 timer

No other combinations are allowed.

Concatenated timers take on the same functionality of a Type B timer.

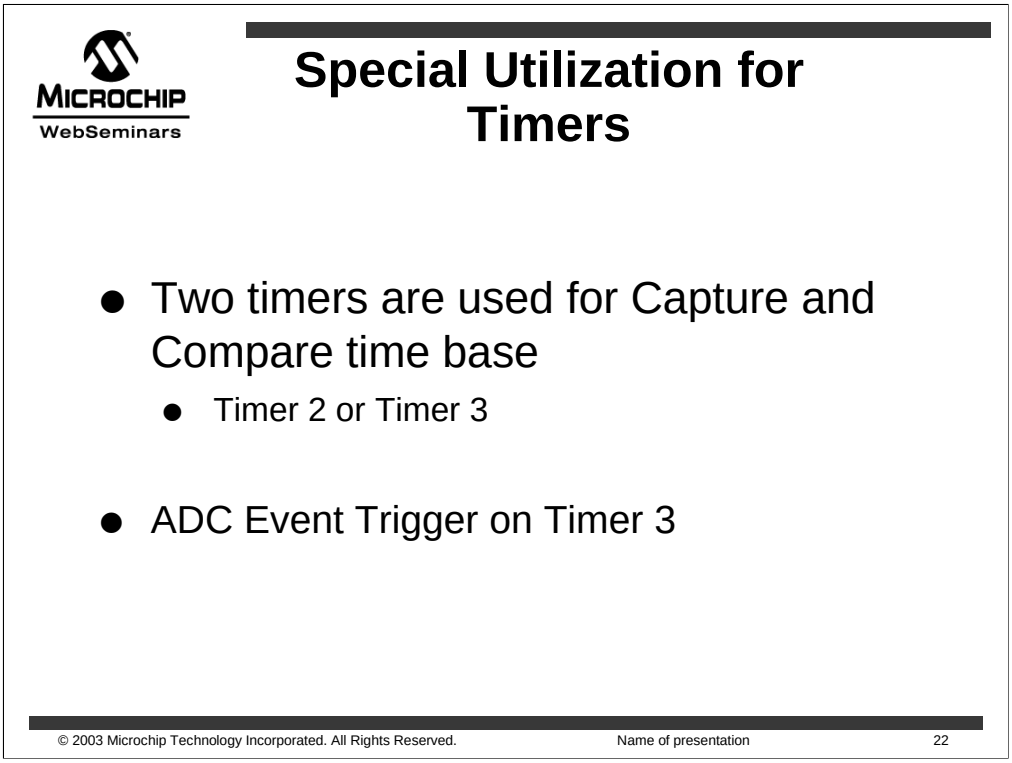


To understand the operation of a 32-bit timer let us take an example of Timer 2 and 3 being concatenated.

The interrupt logic of Timer 3 is used by the combined 32-bit timer. Timer 2 control bits are used and Timer 3 control bits are ignored.

To do a 32-bit read/write operation, a holding register is provided for the 16 most significant bits from Timer 3. When reading the 32-bit timer the user would first read Timer 2. At the instance that timer 2 is read, the timer 3 holding register get loaded with the value in Timer 3. The user then get the most significant 16-bits of Timer3 by reading the timer 3 holding register.

The reverse has be done when doing a 32-bit write. First the timer 3 holding register is loaded with the most significant 16-bit value then a write operation is executed on timer 2 with the least significant 16-bit value. At that instant the value in the timer 3 holding register is loaded into the timer 3 register.



Some special functions of the Timers are listed here.

Timer 2 and timer 3 are used as time bases for the Input Capture and Output Compare modules.

Also Timer 3 can be used as a timer to schedule a start of conversion trigger for an ADC operation, but these are topics for a another time.

Further details of the General purpose Timers and counters can be found in 3 documents, the device data sheet, the dsPIC 30F family reference manual and the dsPIC programmers reference manual. All three documents are needed to fully understand the operations in a dsPIC. As always all our documents are available on our web site www.microchip.com

Thank you for listening and I hope you found this to be time well spent.